Colloque pour les enseignants du secondaire
EPFL STI, 5 novembre 2014, Ecublens

Microélectronique faible consommation : vers des appareils portables de plus grande autonomie et offrant de meilleures performances

Laboratoire d’électronique et de traitement du signal ESPLAB
Pierre-André Farine, Section microtechnique
Microélectronique – Historique

1947 – 1er transistor, W. Schockley

1957 – Technologie planaire

1958 – 1er circuit intégré

1968 – Intel: A. Grove, R. Noyce, G. Moore

1971 – Intel: 1er microprocesseur I4004, µP
Microelectronics – Applications to PDAs, Smart Phones and portable devices

Trends in microelectronics:
- Technology shrinking (14 nm)
- Embedded systems (Size, Weight)
- Enhanced autonomy (Days ... Years)

2013 - Exploded view iPhone 5S

2013 - Tissot Expert Solar and Tissot Lady Solar Touch Screen Technical watches including solar cells
Application domains of microsystems

- Mechanical sensors & detectors (pressure, acceleration, force, ...)
- Actuators (pinches, lockers, levers, ...)
- Motors (linear and rotational, regulated or unregulated)
- Light Emitters (lights, LEDs, EL-Devices, laser diodes, ...)
- Transceivers (visible, infrared, microwaves, radio-frequencies, ...)
- Generators (batteries, rechargeable batteries, Seebeck engines, ...)
- Reactors (Lab-on-a-chip, turbines, ...)
- Microelectronic components for IT/Microsystems/Embedded:
  - Processors (Microprocessors, Microcontrollers, ...)
  - Memories (DRAM, SRAM, Flash-RAM, CD-ROM, Holo-ROM, ...)
  - Communications (USB, Firewire, Bluetooth, Wi-Fi, ...)
  - Displays (CRT, LED, LCD, DMD, OLEDs, ePaper, ...)
  - Man-Machine interfaces (mouse, joystick, track-ball, ...)
Microelectronics – MOS Transistors & μPs

Structural analysis of integrated circuits « 45nm », approaches to obtain the limits of the « nano » performances for silicon devices.

ICs in 2014 : \(10^{19}\) trans. = 10 Exa trans.

Hard disks : \(10^{23}\) bits mem. = 100 Zetta bits
CMOS Technology

• Complementary Metal-Oxide-Semiconductor – CMOS
• First proposed in the 1960s. Was not seriously considered (except by watchmakers!) until the severe limitations in power density and dissipation occurred in n-MOS circuits
• Now the dominant technology in IC manufacturing
• Employs both p-MOS and n-MOS transistors to form logic elements
• The advantage of CMOS is that its logic elements draw significant current only during the transition from one state to another and very little current between transitions - hence power is conserved.
Microelectronics: Low Power CMOS Integrated Circuits

Watches, hearing aids & Portable devices:
- ADC, DAC converters
- DSP microprocessors
- UWB transceivers
- GNSS receivers
- RF circuits
- Baseband systems
Worldwide importance of microtechnology

Microtechnology, worldwide turnover € 30 trillion ($10^{12}$)
Microelectronics, worldwide turnover € 1 trillion
Optics/Photonics, worldwide turnover € 0.1 trillion
Instruments/Devices, worldwide turnover € 0.1 trillion
Watches, worldwide turnover € 30 billion ($10^9$)

1.5 billion watches, 1.5 billion HD drives, 500 million deskjet printers,
300 mio pressure sensors, 100 mio optomagnetic heads,
100 mio optical switches, 100 mio accelerometers,
30 mio gyroscopes, 1 mio beamers ...
Touch Screen Technical Watch

- Interface utilisateur par écran tactile capacitif sur la glace de la montre
- Altimètre, Prévision météo, Température (unités US/EU), Boussole, Chrono, Alarme
- $I = 1.5\mu A$, $V_{DD} = 3V$, $2 \cdot 10^5$ trans.
Swatch Talk II - Watch & GSM dual-band cellular phone

- Analogue Wrist-Watch
- Dual-Band GSM (900 & 1800MHz Cellular Phone)
- Touch Screen User Interface (as in Tissot T-Touch™)
- Fully Waterproof (30m)
- Li-Ion rechargeable battery (400mAh, I = 200mA)
- Talk Time: 2 hours
- Standby Time: 40 hours
- Size: 54x52x24 mm³, 10⁸ tr
- Includes microphone & LP
Salto – Meca Quartz

- High Precision Mechanics
- Analogue Watch with spring barrel + gear train
- Escapement, Balance & Spring removed
- Micro generator, quartz and integrated circuit
- Accuracy : < 1/10 sec/day
- No rechargeable battery, no chemical power supply
- IC : Current cons. I = 80nA
  SOI Techn. V_{DD} = 0.3–0.5V
- -50 à +90° C, 5000 trans.
Power Density available from Harvesters
- How much power is available?

<table>
<thead>
<tr>
<th>PV</th>
<th>TEG</th>
<th>PE</th>
<th>RF</th>
</tr>
</thead>
<tbody>
<tr>
<td>![PV Image]</td>
<td>![TEG Image]</td>
<td>![PE Image]</td>
<td>![RF Image]</td>
</tr>
<tr>
<td>Outdoor 10'000 μW/cm²</td>
<td>Man 20 μW/cm²</td>
<td>Man 4 μW/cm²</td>
<td>GSM 0.1 μW/cm²</td>
</tr>
<tr>
<td>Indoor 10 μW/cm²</td>
<td>Machine 10'000 μW/cm²</td>
<td>Machine 100 μW/cm²</td>
<td>WiFi 0.01 μW/cm²</td>
</tr>
</tbody>
</table>

Source: S. Roundy, Kluwer, 2004
MOSFET – Metal Oxyde Semiconductor Field Effect Transistor

[Sze]
MOS diode - Energy band diagram at $V = 0$

[Sze]
Ideal MOS diode - Energy Band diagrams and charge distributions – 3 cases

(a) accumulation

(b) depletion

(c) inversion

c1) Weak inversion: $\Psi_B < \Psi_S < 2\Psi_B$
c2) Strong inversion: $\Psi_S \geq 2\Psi_B$

[Sze]
MOSFET - $I_D = f(V_D)$ & $I_D = f(V_G)$

Idealized drain characteristics $I_D = f(V_D)$

Transfer characteristics in linear region $I_D = f(V_G)$

[Sze]
Layout of a conventional MOS transistor
DIGITAL CMOS IC INVERTER: CIRCUIT LAYOUT

Complementary MOS inverter.

(a) Circuit diagram
(b) Circuit layout.
(c) Cross section along dotted A-A’ line of (b). [Sze]
EPROM, EEPROM & Flash Memory
Basic Operation Principle

Storage of charges

Gate

Source

n^+

n^+

P -sub

Drain

Q_T

Gate Voltage, \( V_{GS} \)

Erased

Programmed

Darin Current

Sense voltage
CMOS Technology Scaling

1. CMOS scaling driven by digital applications
   • Memories: high density and low power constraints
   • Microprocessors: high performance and speed

2. Analog use a digital process as bare bones baseline

3. Huge implications on analog design, creating new challenges as silicon continues to scale down, including headroom, gain, leakage, variations, mismatches and automated CAD

[ Bergemont, 2012 ]
Moore’s Law – Predictions for 2010-2019

ITRS - International Technology Roadmap for Semiconductors
In 2014, CMOS technology with 14 nm design rules ($L_G = 6\text{nm}$)
# International Technology Roadmap for Semiconductors

**ITRS for Deep Submicron CMOS Technologies**

<table>
<thead>
<tr>
<th></th>
<th>2007</th>
<th>2010</th>
<th>2013</th>
<th>2016</th>
<th>2019</th>
</tr>
</thead>
<tbody>
<tr>
<td>Technology node (nm)</td>
<td>65</td>
<td>45</td>
<td>32</td>
<td>22</td>
<td>16</td>
</tr>
<tr>
<td>Gate length $L_G$ (nm)</td>
<td>25</td>
<td>18</td>
<td>13</td>
<td>9</td>
<td>6</td>
</tr>
<tr>
<td>Voltage supply (V)</td>
<td>1.1</td>
<td>1.0</td>
<td>0.9</td>
<td>0.8</td>
<td>0.7</td>
</tr>
<tr>
<td>Dielectric equivalent thickness (nm)</td>
<td>1.8</td>
<td>1.1</td>
<td>1.0</td>
<td>0.9</td>
<td>0.9</td>
</tr>
<tr>
<td>Threshold voltage $V_{TH}$ (V)</td>
<td>0.165</td>
<td>0.167</td>
<td>0.185</td>
<td>0.195</td>
<td>0.205</td>
</tr>
<tr>
<td>Leakage current ($\mu$A/$\mu$m)</td>
<td>0.20</td>
<td>0.22</td>
<td>0.11</td>
<td>0.11</td>
<td>0.11</td>
</tr>
<tr>
<td>On state current ($\mu$A/$\mu$m)</td>
<td>1200</td>
<td>1815</td>
<td>2220</td>
<td>2713</td>
<td>2744</td>
</tr>
<tr>
<td>NMOS delay – $CV/I$ (ps)</td>
<td>0.640</td>
<td>0.400</td>
<td>0.250</td>
<td>0.150</td>
<td>0.100</td>
</tr>
</tbody>
</table>
Physical Limits in Microelectronics

Gate length: \( L_G = 0.0065 \mu m = 65 \text{ nm} \), \( L_G \)

(limit: \( L_G = \hbar / \Delta p = 1.5 \text{ nm} \))

Voltage supply: \( V_{dd} = 0.5V \)

(limit: \( V = k \cdot T/q = 25 \text{ mV}, T = 300K \))

Parasitic Capacity: \( C = 1 \text{ fF} \)

(limit: \( C = q^2/k \cdot T = 6.4 \cdot 10^{-3} \text{ fF} \))

Energy/operation: \( E = C \cdot V^2 = 0.25 \text{ pJ} \)

(limit: \( E = k \cdot T \cdot \ln 2 = 2.8 \cdot 10^{-21} \text{ J} \))

Electrons count: \( n = C \cdot V / q = 3'125 \text{ e}^- \)

(limit: \( 1 \text{ e}^-, t_{min} = \hbar / \Delta E = 0.04 \text{ ps} \))

Maximal Density: \( 1 / L_G^2 = 4.7 \cdot 10^{13} \text{ tr/cm}^2 \)

\( P_{max} = 3.7 \cdot 10^6 \text{ W/cm}^2 \)
CMOS Technology Scaling – The Dilemma

V_{DD} Scaling

Lower Cost
Less Leakage
Less Power

Do NOT Scale!!

Less SNR,
Less Accuracy,
More Power

\[ P \propto f C V_{DD}^2 + I_{\text{leak}} V_{DD} \]

Colloque pour les enseignants des gymnases
5 novembre 2014

[ Bergemont, 2012 ]
MOSFET: Hot Electron Effects

1. Injection and trapping → Instability
2. Avalanche multiplication → Holes
3. Substrate Current → Polarization of substrate
4. Injection of electrons → Current leakage and breakdown
5. Bipolar transistor effects → Current leakage and breakdown
The CMOS Power Crisis

- As transistor density has increased, the supply voltage ($V_{DD}$) has not decreased proportionately.
  
  $\Rightarrow$ Power density now constrains CMOS chip design!

![CMOS Voltage Scaling](image1)

![Power Density vs. Gate Length](image2)

Source: P. Packan (Intel), 2007 IEDM Short Course

Source: B. Meyerson (IBM), Semico Conf., January 2004
Sources of Variability

- Sub-wavelength lithography:
  - Resolution enhancement techniques are costly and increase process sensitivity

- Layout-dependent transistor performance:
  - Process-induced stress is dependent on layout

- Random dopant fluctuations (RDF):
  - Atomistic effects become significant in nanoscale FETs


CMOS Technology Scaling

XTEM images with the same scale
courtesy V. Moroz (Synopsys, Inc.)

90 nm node  65 nm node  45 nm node  32 nm node

- Gate length has not scaled proportionately with device pitch (0.7x per generation) in recent generations.
  - Transistor performance has been boosted by other means.

[King Liu]
MOSFET Performance Boosters

- Strained channel regions $\rightarrow \mu_{\text{eff}} \uparrow$
- High-k gate dielectric and metal gate electrodes $\rightarrow C_{\text{ox}} \uparrow$

Cross-sectional TEM views of Intel’s 32nm CMOS devices

P. Packan et al., IEDM Technical Digest, pp. 659-662, 2009

[King Liu]
Effects of Random Dopant Fluctuations RDF

✓ RDF Random Dopant Fluctuations getting worse as less dopants in the channel

Discrete dopants randomly distributed in (Xnm)$^3$ cubes with average conc of 5X10$^{18}$ cm$^3$

✓ 5000 dopants within (100nm)$^3$ cube
✓ Average 40 dopants within its 125 sub-cubes of (20nm)$^3$

✓ At minimum $L$, control and variations are exacerbated, mainly through $V_t$
  - $V_t$ dependence on $V_ds$ getting worse (SCE)
  - Better control with large $W$

NMOS $V_T$ & Ioff [L down to 20nm for (a) width=200nm and (b) width=20nm at $V_d=1.0V$ (Source TSMC)]

[Source: Bergemont]
Gate Leakage

• Mechanism is tunneling through thin gate oxide.
• Gate leakage extremely sensitive to the oxide thickness.
• 65nm node shifted the leakage by more than six orders of magnitude as compared to 0.18 um node

For digital circuits, power associated with gate leakage is acceptable until oxide thickness reduces less than 2nm (~1A/cm2)
• When high-κ materials are used as the gate insulator in later generation devices, gate leakage currents are greatly reduced.

[Bergemont]
Structures to resolve lateral leakage

✓ ISSUE

drain control competing with gate control

✓ SOLUTIONS

Provide gate control from more than one side of the channel (Multi-gate FETs)

Vertical gates: FINFET

Channel consists of two vertical surfaces and the top surface of the fin (Intel)

Lateral Gates: UTSoI

FDSOI with back planes

Fully Depleted Silicon On Insulator (ST 28nm)
Conclusions - MOSFET Evolution

32 nm planar $\rightarrow$ 22 nm multi-gate segmented channel $\rightarrow$ beyond 10 nm stacked nanowires?

Stacked gate-all-around (GAA) FETs achieve the highest layout efficiency.

[King Liu]
Chip Scale Cs Atomic Clock

- VCSEL thermal stabilization
- CELL thermal stabilization
- Low-noise photodetection
- VCSEL optical frequency control (servo loop)
- 4.6 GHz RF synthesis
- CPT signal amplification and VCXO servo-loop
- Light shift control through RF power servo-loop
- C-field control through Zeeman interrogation
Merci pour votre attention !
Some References

• A. Bergemont, “Lessons from 15 years of fab development for deep sub-micron mixed signal ICs”, IEEE Swiss Chapter, March 2012
• T. J. King Liu, “Bulk CMOS Scaling to the End of the Roadmap”, Symposium on VLSI Circuits Short Course, UC Berkeley, June 2012